CLAIMS

We claim:

1. A method for facilitating high signal throughput of an improved CMOS image sensor comprising a plurality of photo sensors configured in a two-dimensional array; said method comprising:

generating column address signals and row address signals that address a subset of said two-dimensional array according to a set of parameters; and

reading out charge signals from a set of the plurality of photo sensors in said image sensor; said set of photo sensors addressed by said column address signals and said row address signals.

2. The method as recited in claim 1 wherein said reading out charge signals comprises:

shifting said charge signals from said set of the plurality of photo sensors, respectively, to line buses in parallel;

3. The method as recited in claim 2 further comprising:

conditioning said charge signals to appropriate levels before being digitized in parallel in a bank of analog-to-digital converters to produce pixel signals; and

processing said pixel signals with respect to instructions from a memory;

4. The method as recited in claim 3 wherein said processing said pixel signals is carried out in a pixel processor.

5. The method as recited in claim 4 wherein said pixel processor and said memory are monolithically integrated with said plurality of photo sensors of the CMOS image sensor.

6. The method as recited in claim 3 wherein said conditioning said charge signals comprises balancing colors in said charge signals.

7. The method as recited in claim 6 wherein said balancing colors comprises:

deriving a measurement difference of each of said charge signals with a reference; and

adjusting said each of said charge signals with respect to said measurement difference.

8. The method as recited in claim 2 further comprising generating an optimum exposure time.

9. The method as recited in claim 8 wherein said generating an optimum exposure time comprises:

deriving a measurement difference of each of said charge signals with a reference; and

calculating said optimum exposure time from said measurement difference.

10. The method as recited in claim 1, wherein said set of parameters includes coordinates of a region of interest and wherein said generating column signals and row signals comprises:

identifying said set of the plurality of photo sensors corresponding to said coordinates of said region of interest;

11. The method as recited in claim 10 wherein said processing pixel signals comprises producing a larger set of digital signals by interpolating said pixel signals.

12. The method as recited in claim 10 wherein said processing pixel signals comprises:

detecting if said charge signals represent an image of a target being focused; and

producing a reference signal to cause said image sensor to regenerate said charge signals with a new setting if said detecting indicates said target is not represented well in said image.

13. A method for facilitating high signal throughput of an improved CMOS image sensor comprising a plurality of photo sensors configured in a two-dimensional area; said method comprising:

reading out charge signals from said plurality of photo sensors row by row in parallel to respective column buses; said column buses coupled to a double sampling circuit and a programmable gain amplifier;

conditioning said charge signals in said programmable gain amplifier in accordance with said double sampling circuit before said charge signals are digitized to produce pixel signals; and

processing said pixel signals in a pixel processor to produce a desired result.

14. The method as recited in claim 13 wherein said pixel processor, said double sampling circuit and said programmable gain amplifier are monolithically integrated with said plurality of photo sensors of the CMOS image sensor.

15. The method as recited in claim 13 wherein said conditioning said charge signals comprises:

deriving a measurement difference of each of said charge signals with a reference in said double sampling circuit; and

adjusting said each of said charge signals with respect to said measurement difference said programmable gain amplifier.

16. The method as recited in claim 13 wherein said desired result is a compressed format of said pixel signals and wherein said processing said pixel signals in a pixel

processor comprises compressing said pixel signals according to a commonly used compression standard.

17. The method as recited in claim 16 wherein the commonly used compression standard is selected from a group consisting of Graphic Interchange Format (GIF), JPEG (Joint Photographic Experts Group) and MPEG (Moving Picture Experts Group) supported by a World Wide Web protocol.

18. The method as recited in claim 13 wherein said desired result is a gray-scale intensity image and wherein said processing said pixel signals in a pixel processor comprises converting said pixel signals respectively to intensity data according to a predefined conversion standard.

19. An architecture for facilitating high signal throughput of an improved CMOS image sensor comprising a plurality of photo sensors configured in a two-dimensional area; said architecture comprising:

a pair of column address and row address decoders providing address signals to address each of the plurality of photo sensors;

a number of signal conditioning circuits, each coupled to a column data bus receiving charge signals readout from said photo sensors when said photo sensors are addressed by said address signals;

a number of analog-to-digital converters, each respectively coupled to one of said conditioning circuits and digitizing said charge signals in parallel; to produce pixel signals; and

a pixel processor receiving said pixel signals from said analog-to-digital converters, wherein said pixel signals are processed to produce a desired result.

20. The architecture as recited in claim 19 wherein each of the signal conditioning circuits comprises a correlated double sampling circuit and a programmer gain amplifier.

21. The architecture as recited in claim 20 wherein said correlated double sampling circuit derives a measurement difference of each of said charge signals with a reference.

22. The architecture as recited in claim 21 wherein said programmer gain amplifier receives said measurement difference and adjusts said each of said charge signals with respect to said measurement difference.

23. The architecture as recited in claim 21 wherein each of the signal conditioning circuits produces a signal that indicates an optimum exposure time.

24. The architecture as recited in claim 23 wherein said correlated double sampling circuit and said programmer gain amplifier together derives a measurement difference of each of said charge signals with a reference; and calculates said optimum exposure time from said measurement difference.

25. The architecture as recited in claim 20 further comprises a memory storing instructions; said memory coupled to said pixel processor that executes said instructions from said memory to achieve said desired result.

26. The architecture as recited in claim 25 wherein said instructions causes said pixel processor to compress said pixel signals according to a commonly used compression standard.

27. The architecture as recited in claim 26 wherein the commonly used compression standard is selected from a group consisting of Graphic Interchange Format (GIF), JPEG (Joint Photographic Experts Group) and MPEG (Moving Picture Experts Group) supported by a World Wide Web protocol.

28. The architecture as recited in claim 25 wherein said instructions causes said pixel processor to convert said pixel signals respectively to intensity data according to a predefined conversion standard.

29. The architecture as recited in claim 19 wherein said pixel processor is monolithically integrated with said photo sensors.

30. The architecture as recited in claim 20 wherein said pixel processor, said correlated double sampling circuit and said programmer gain amplifier are is monolithically integrated with said photo sensors.